Amendments to the Claims:

This listing of Claims will replace all prior versions, and listings, of claims in the application where added material is shown in underlined type, deleted material is shown in ~~strikeout type~~ or within double brackets:

Listing of Claims:

Claims 1-181 (Canceled)

182. (New) A system for adaptive configuration, the system comprising:

a memory adapted to store configuration information including a first configuration information and a second configuration information;

a first computational unit having a configurable basic architecture including a first plurality of heterogeneous computational elements and a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together, the first interconnection network configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function; and

a second computational unit having a configurable complex processing architecture including a second plurality of heterogeneous computational elements and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together, the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function.

183. (New) The system of claim 182, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

184. (New) The system of claim 182, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information.

185. (New) The system of claim 182, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information.

186. (New) The system of claim 182, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface.

187. (New) The system of claim 182, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits.

188. (New) The system of claim 182, wherein the system is embodied within an integrated circuit.

189. (New) The system of claim 182, wherein the computational units are organized in a configurable computing matrix and the computing matrix is coupled to a matrix interconnection network.

190. (New) The system of claim 189, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of computational units.

191. (New) The system of claim 189, wherein a first configured function of the configurable computing matrix is as a controller.

192. (New) The system of claim 190, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices.

193. (New) The system of claim 191, wherein the controller is a RISC controller.

194. (New) The system of claim 182, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

195. (New) The system of claim 194, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

196. (New) The system of claim 182, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

197. (New) The system of claim 182, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

198. (New) The system of claim 182, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

199. (New) The system of claim 198, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

200. (New) The system of claim 199, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

201. (New) The system of claim 197, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

202. (New) The system of claim 196, wherein the first computational unit operates at a bit level; and

wherein the second computational unit operates at a word level.

203. (New) The system of claim 202, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

204. (New) The system of claim 182, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions.

205. (New) The system of claim 204, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

206. (New) The system of claim 205, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

207. (New) The system of claim 206, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a

function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

208. (New) The system of claim 207, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

209. (New) The system of claim 182, further comprising a third interconnection network coupled to the first computational unit and the second computational unit, the third interconnection network sending the configuration information to the computational units.

210. (New) The system of claim 209, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

211. (New) The system of claim 182, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements.

212. (New) The system of claim 211, wherein the configuration information includes control signals to control the multiplexers.

213. (New) A system for adaptive configuration, the system comprising:

a memory adapted to store configuration information including a first configuration information and a second configuration information;

a first configurable basic computational logic unit including a first plurality of heterogeneous computational elements and a first interconnection network for forming a first configurable architecture, the first interconnection network configurably coupling the first plurality of heterogeneous computational elements together; the first interconnection network

configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function; and

a second configurable complex processing unit including a second plurality of heterogeneous computational elements and a second interconnection network for forming a second configurable architecture, the second interconnection network configurably coupling the second plurality of heterogeneous computational elements together; the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function.

214. (New) The system of claim 213, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

215. (New) The system of claim 213, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information.

216. (New) The system of claim 213, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information.

217. (New) The system of claim 213, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface.

218. (New) The system of claim 213, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits.

219. (New) The system of claim 213, wherein the system is embodied within an integrated circuit.

220. (New) The system of claim 213, wherein the logic unit and processing unit are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

221. (New) The system of claim 220, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of logic and processing units.

222. (New) The system of claim 213, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

223. (New) The system of claim 220, wherein a first configured function of the configurable computing matrix is as a controller.

224. (New) The system of claim 221, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices.

225. (New) The system of claim 223, wherein the controller is a RISC controller.

226. (New) The system of claim 213, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

227. (New) The system of claim 226, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

228. (New) The system of claim 213, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

229. (New) The system of claim 213, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

230. (New) The system of claim 213, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

231. (New) The system of claim 230, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

232. (New) The system of claim 231, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

233. (New) The system of claim 229, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

234. (New) The system of claim 228, wherein the first configurable basic computational logic unit operates at a bit level; and

wherein the second configurable complex processing unit operates at a word level.

235. (New) The system of claim 234, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

236. (New) The system of claim 213, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions.

237. (New) The system of claim 236, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

238. (New) The system of claim 237, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

239. (New) The system of claim 238, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

240. (New) The system of claim 239, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

241. (New) The system of claim 213, further comprising a third interconnection network coupled to the first configurable basic computational unit and the second configurable complex processing unit, the third interconnection network sending the configuration information to the units.

242. (New) The system of claim 241, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

243. (New) The system of claim 213, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements.

244. (New) The system of claim 243, wherein the configuration information includes control signals to control the multiplexers.

245. (New) The system of claim 213, wherein the first interconnection network provides a third configuration information to reconfigure the first configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.

246. (New) A method for adaptive configuration of an integrated circuit, the method comprising:

receiving configuration information;

storing the configuration information in a memory; and

in response to the configuration information:

configuring interconnections between a first plurality of heterogeneous computational elements of the integrated circuit via a first interconnection network of the integrated circuit to provide a configurable basic computational unit to perform a basic computational function, the first interconnection network configurably coupling the first plurality of heterogeneous computational elements together; and

configuring interconnections between the second plurality of heterogeneous computational elements of the integrated circuit via the second interconnection network of the integrated circuit to provide a configurable complex computational unit to perform a complex processing function, the second interconnection network configurably coupling the second plurality of heterogeneous computational elements together.

247. (New) The method of claim 246, further comprising requesting authorization to receive the configuration information.

248. (New) The method of claim 246, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

249. (New) The method of claim 246, wherein the configuration information is received from a machine-readable medium or via a wireless interface.

250. (New) The method of claim 246, wherein the computational units are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

251. (New) The method of claim 250, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of computational units.

252. (New) The method of claim 246, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

253. (New) The method of claim 250, wherein a first configured function of the configurable computing matrix is as a controller.

254. (New) The method of claim 251, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices.

255. (New) The method of claim 253, wherein the controller is a RISC controller.

256. (New) The method of claim 246, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

257. (New) The method of claim 250, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

258. (New) The method of claim 246, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

259. (New) The method of claim 246, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

260. (New) The method of claim 246, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a

function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

261. (New) The method of claim 260, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

262. (New) The method of claim 261, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

263. (New) The method of claim 259, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

264. (New) The method of claim 258, wherein the configurable basic computational logic unit operates at a bit level; and

wherein the configurable complex processing unit operates at a word level.

265. (New) The method of claim 264, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

266. (New) The method of claim 246, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions.

267. (New) The method of claim 266, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

268. (New) The method of claim 267, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

269. (New) The method of claim 268, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

270. (New) The method of claim 269, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

271. (New) The method of claim 246, further comprising a third interconnection network coupled to the configurable basic computational unit and the configurable complex computational unit, the third interconnection network sending the configuration information to the units.

272. (New) The method of claim 271, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

273. (New) The method of claim 246, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements.

274. (New) The method of claim 273, wherein the configuration information includes control signals to control the multiplexers.

275. (New) The method of claim 246, wherein the first interconnection network provides a third configuration information to reconfigure the configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.

276. (New) A method for adaptive configuration of an integrated circuit, the integrated circuit having a first plurality of heterogeneous computational elements, a second plurality of heterogeneous computational elements, and an interconnection network coupled to the memory, the interconnection network having and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together, the method comprising:

transmitting configuration information;

wherein the configuration information is received;

storing the received configuration information in a memory; and

in response to the configuration information:

configuring interconnections between a first plurality of heterogeneous computational elements via a first interconnection network to provide a configurable basic computational unit to perform a basic computational function, the first interconnection network configurably coupling the first plurality of heterogeneous computational elements together; and

configuring interconnections between a second plurality of heterogeneous computational elements via a second interconnection network to provide a configurable complex computational unit to perform a complex processing function, the second interconnection network configurably coupling the second plurality of heterogeneous computational elements together.

277. (New) The method of claim 276, further comprising requesting authorization to receive the configuration information.

278. (New) The method of claim 276, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

279. (New) The method of claim 276, wherein the configuration information is received from a machine-readable medium or via a wireless interface.

280. (New) The method of claim 276, wherein the computational units are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

281. (New) The method of claim 280, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrices, each configurable computing matrix having a plurality of computational units.

282. (New) The method of claim 276, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

283. (New) The method of claim 280, wherein a first configured function of the configurable computing matrix is as a controller.

284. (New) The method of claim 281, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrices.

285. (New) The method of claim 283, wherein the controller is a RISC controller.

286. (New) The method of claim 276, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

287. (New) The method of claim 286, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

288. (New) The method of claim 276, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

289. (New) The method of claim 276, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

290. (New) The method of claim 276, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

291. (New) The method of claim 290, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

292. (New) The method of claim 291, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

293. (New) The method of claim 289, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

294. (New) The method of claim 288, wherein the configurable basic computational logic unit operates at a bit level; and

wherein the configurable complex processing unit operates at a word level.

295. (New) The method of claim 294, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

296. (New) The method of claim 276, wherein the basic computational function includes one of a group of linear operation, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic functions, floating point arithmetic functions, filter functions, and transformation functions.

297. (New) The method of claim 296, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

298. (New) The method of claim 297, wherein the basic computational function comprises it level manipulation; and

wherein the complex processing function comprises word level manipulation.

299. (New) The method of claim 297, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a

function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

300. (New) The method of claim 299, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

301. (New) The method of claim 276, further comprising a third interconnection network coupled to the configurable basic computational unit and the configurable complex computational unit, the third interconnection network sending the configuration information to the units.

302. (New) The method of claim 301, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

303. (New) The method of claim 276, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements, and the second interconnection network includes other multiplexers coupled to the second plurality of heterogeneous computational elements.

304. (New) The method of claim 303, wherein the configuration information includes control signals to control the multiplexers.

305. (New) The method of claim 276, wherein the first interconnection network provides a third configuration information to reconfigure the configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.